Quantum Confinement in Si-channel Nanowire MOSFETs

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***Abstract*—Gate-all-around nanowire MOSFETs exhibit excellent gate control of the channel. However, quantum confinement in Silicon channel moves peak electron concentration away from oxide/Silicon interface. This reduces on-state current of the MOSFETs. Quantum effects are not readily taken into account in the drift-diffusion framework. Various models have been developed to include these effects in the framework. SemiVi drift-diffusion simulator models quantum confinement effects using Van-Dort, modified local density approximation, and density gradient models.**

***Index Terms*—Nanowire MOSFETs, Silicon, quantum confinement, mobility degradation.**

I. Introduction

Silicon channel FinFET scaling has reached its limit. Further scaling can be achieved by changing the device geometry from FinFET to a Gate-all-around (GAA) nanowire FET. In this work, one such GAA-FET is studied by TCAD simulations using SemiVi drift-diffusion solver. Quantum confinement in the channel moves peak electron (hole) concentration in n-FET (p-FET) away from oxide/Silicon interface. This degrades gate control of the channel and also reduces On-current. This work models quantum confinement using three different models available in the literature - Van Dort model, Modified Local Density Approximation (MLDA) model, and Density Gradient method.

II. Modeling quantum confinement

A. Van Dort model

In this model, quantum potential is defined as follows.

$$\Lambda_{n/p} = -\frac{13}{9} \cdot \beta \cdot f(|\vec{r}|) \cdot \left(\frac{\epsilon_r \cdot \epsilon_0}{4 \cdot \mathrm{kT}}\right)^{1/3} \cdot \left(F_\perp - F_{\mathrm{crit}}\right)^{2/3} \quad (1)$$

where ϵ_r relative permittivity of the semiconductor, ϵ_0 is permittivity of free space, kT thermal voltage, $F_\perp$ is local electric field normal to the nearest oxide/semiconductor interface. The parameters β and F_{crit} are calibration parameters. $f(|\vec{r}|)$ is a function of the distance of the vertex from the interface, given by.

$$f(x) = \frac{2\exp(-\frac{x}{l_{\mathrm{ref}}})}{1+\exp(-\frac{x}{l_{\mathrm{ref}}})} \quad (2)$$

B. MLDA model

In this model, quantum potential is defined at each vertex in the region as follows.

$$\Lambda_{n/p} = \log\left(1 - \exp(-\frac{d_\perp}{\lambda_{n/p}})\right) \quad (3)$$

Here, $d_\perp$ is the distance of the vertex from nearest insulator/semiconductor interface and $\lambda_{n/p}$ is thermal wavelength given by,

$$\lambda_{n/p} = \sqrt{\frac{\hbar^2}{2 \cdot kT \cdot m_{\mathrm{n/p}}}} \quad (4)$$

Here, $m_{\mathrm{n/p}}$ is the quantum confinement mass which is taken as a fitting parameter.

C. Density Gradient Equation

In this approach, quantum potential is defined by a function of the gradient of carrier density, hence the name density gradient. In this approach, quantum potential is defined as,

$$\Lambda_n = -\frac{\hbar^2}{6 \cdot m_n \cdot q}\frac{\nabla^2\sqrt{n}}{\sqrt{n}} \quad (5)$$

$$= -\frac{\gamma\hbar^2}{12 m_{\mathrm{e}} q}\left(\nabla^2 \ln n + \frac{1}{2}(\ln n)^2\right) \quad (6)$$

Here, $m_{n/p}$ is the quantization effective mass, m_e is free electron mass, n is electron density. In second part of Eq. 5, the quantized effective mass is replaced by a fitting parameter γ.

Defining electron density with Boltzmann distribution ($n = n_i \exp\left(\frac{\psi+\Lambda_n-\phi_n}{kT/q}\right)$), Eq. 5 can be reformulated as follows.

$$\Lambda_n = -\frac{\gamma\hbar^2}{12 m_{\mathrm{e}} q}\left(\nabla^2 u + \frac{1}{2}(\nabla u)^2\right) \quad (7)$$

where $u = \frac{\psi+\Lambda_n-\phi_n}{kT/q}$. Notice, that the solution term Λ_n exists on both sides of Eq. 7. Additionally, RHS of Eq. 7 depends on logarithm of electron density n, whereas n depends on Λ_n. Hence, the above equation must be solved together with Poisson and carrier continuity equation.

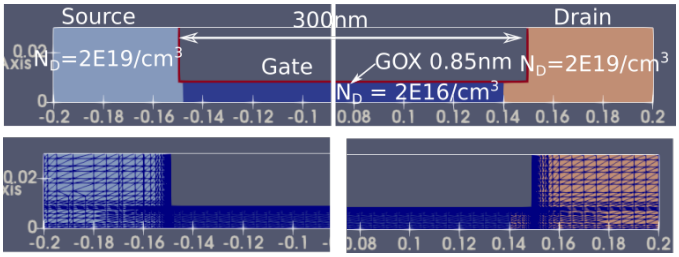


Fig. 1. (a) Structure and mesh of the simulated n-MOSFET with L_G = 300nm. Similar p-MOSFET with p-source and drain is simulated. (b) Dopant distribution in the simulated device with L_G = 300nm.

III. Simulation Setup

A. Device structure

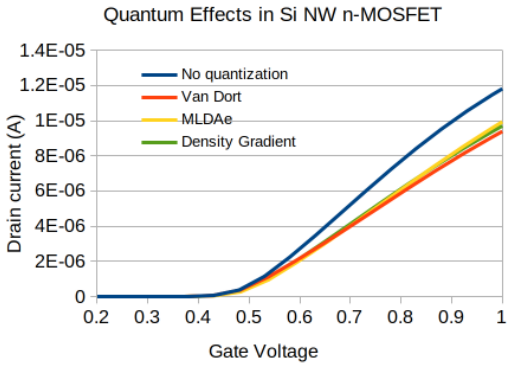
The Si nanowire MOSFETs simulated in this work were fabricated using a CMOS-compatible self-aligned replacement-metal-gate process. The fabrication process is described in [**?**] and [**?**]. The process is designed to fabricate ultra-thin-body MOSFETs with variable widths. Here, we have selected the MOSFETs with 500nm width for the simulation. Since the MOSFET structure is invariant along the width, 2D cross-section of the MOSFET with L_G = 13nm, 100nm, and 300nm are generated and meshed by using SemiVi structure generator and mesher [1]. The device structure and the doping profiles of L_G = 13nm MOSFET are shown in Fig. III-A. Channel region of the MOSFET is intrinsically n-doped with doping of $2 \times 10^{16}\,\mathrm{cm}^{-3}$, whereas raised- source and drain regions are heavily n-doped. The gate-oxide is a high-k oxide with an equivalent oxide thickness (EOT) of 8.5Å.

The Si nanowire p- and n-MOSFETs are simulated in this work using cylindrical coordinate system. 2D radial cross-sections of the devices with L_G = 300nm are created using SemiVi structure generator and mesher [1]. These devices are simulated using SemiVi drift-diffusion solver [2] with the Cylindrical coordinate system. The device structure and the doping profiles of L_G = 300nm n-MOSFET are shown in Fig. III-A. Channel-region of both p- and n-MOSFET is n-doped with doping of $2 \times 10^{16}\,\mathrm{cm}^{-3}$, whereas raised-source and drain regions are heavily n- or p-doped in n- or p-MOSFETs, respectively. Gate-oxide is modeled as SiO_2 with an equivalent oxide thickness (EOT) of 8.5Å.

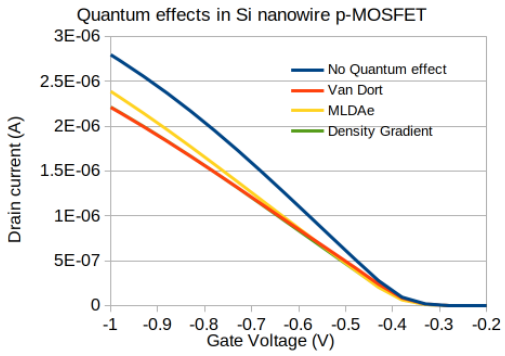
B. Simulation parameters

In this work, bulk electron and hole mobility in Silicon is set to 1450 cm^2/Vs and 450 cm^2/Vs, respectively. Channel mobility degradation is modeled using "Lombardi model". Electron and hole lifetimes in the material are set to 1μsec.

Quantum confinement moves electron density away from the GOX/Silicon interface. This effect is modeled in the drift-diffusion simulations using three different models - Van Dort model, modified local density approximation (MLDA), and density gradient model.



(a) n-MOSFET



(b) p-MOSFET

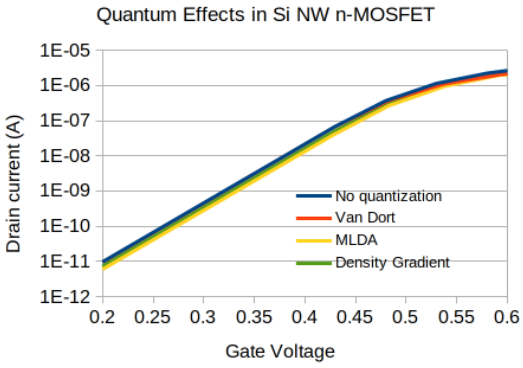
Fig. 2. Simulated transfer characteristics of Silicon nanowire (a) n-MOSFET, and (b) p-MOSFET with L_G =300nm showing the quantum effects modeled by the three different models.

IV. Results

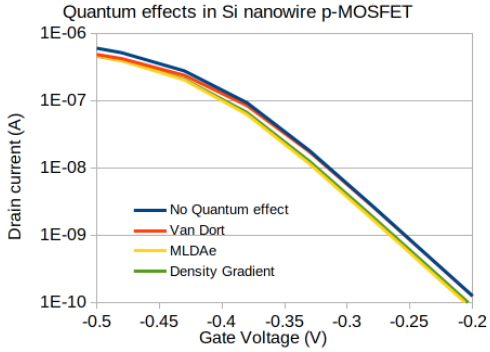
Comparison of the simulated transfer characteristics of the nanowire p- and n-MOSFETs with the measurements is shown in Fig. 2(a) and Fig. 2(b), for n- and p-MOSFETs of L_G = 300nm, respectively. The figures show that on-state current is reduced when quantum confinement is taken into account. This is due to redistribution of carrier density due to quantum effects. In the on-state, electron (hole) density in nMOSFET (pMOSFET) shifts away from GOX/Si interface. This is shown in Fig. 4. Transfer characteristics are plotted on semilog-y scale in Fig. 3(a) and Fig. 3(b) to highlight the subthreshold region.

References

[1] Structure Generator and Mesher User Guide, SemiVi LLC, Switzerland, 2025.
[2] Drift-diffusion Solver User Guide, SemiVi LLC, Switzerland, 2025.
[3] C. Lombardi et al., "A Physically Based Mobility Model for Numerical Simulation of Non-planar Devices," IEEE Trans. Computer-Aided Design, vol. 7, no. 11, pp. 1164-1171, 1988.



(a) n-MOSFET



(b) p-MOSFET

Fig. 3. Simulated transfer characteristics of Silicon nanowire (a) n-MOSFET, and (b) p-MOSFET showing the quantum effects in the subthreshold region.

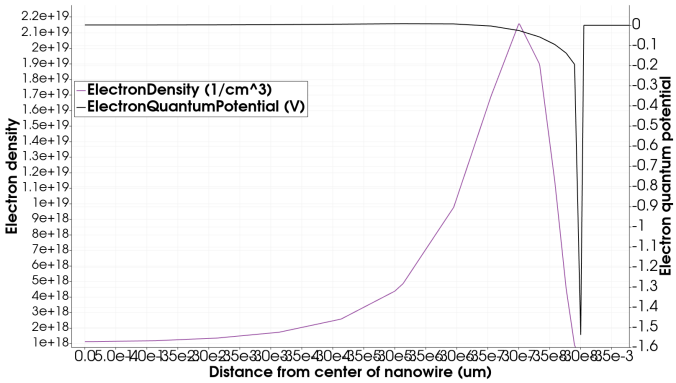


Fig. 4. Quantum potential and electron density are plotted perpendicular to GOX/Silicon interface at x=0. Right part after the peak is oxide, that before the peak is Silicon. Quantum potential is highest at GOX/Si interface. Quantum potential is simulated using density gradient approach.