

Effect of interface traps on a double-gate MOSFET

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Abstract—Effect of traps at gate-oxide/Silicon interface of double-gate n- and p-channel MOSFETs is studied using SemiVi drift-diffusion solver. Mobility degradation due to interface roughness, doping, and high-field mobility saturation is taken into account in the simulations. Transfer characteristics of the MOSFETs with different trap concentration are compared to analyze the effect of interface traps.

Index Terms—Double-gate MOSFET, drift-diffusion, FinFET.

I. INTRODUCTION

Modern FinFETs use a thoroughly engineered gate-oxide stack of high-k dielectric together with SiO₂. Although this gate-oxide engineering achieves strong gate control of the channel, it results in defect formation at oxide/Silicon channel interface. These defects (also called traps) can potentially shield channel from the gate, thereby weakening the gate control of the channel.

In this work, we perform simulation study of n- and p-channel double-gate MOSFET (DG-MOSFET) to obtain transfer characteristics with and without oxide/Silicon traps. Additionally, trap density at the interface is varied to study its effect on the transfer characteristics.

II. MOBILITY DEGRADATION IN NANO-SCALE MOSFET

As the source and the drain regions are heavily doped, resistance of a MOSFET often depends on the channel resistance. Presence of impurities in the channel region increases scattering resulting in channel mobility degradation. In the SemiVi simulator, this is modeled by activating Masetti model throughout the device.

Silicon/Gate-oxide interface often exhibits roughness, which adds to scattering of carriers in the inversion layer. This degrades mobility of the carriers in the channel. This, surface-roughness induced mobility degradation is modeled by a model proposed by Lombardi et al.

Carrier velocity is given by $\vec{v} = \mu \cdot \vec{F}$, where $\vec{F}$ is electric field. $\vec{v}$ increases with $\vec{F}$. But this increase is sub-linear, and saturates at high fields. This is due to the increased scattering at high electric field. This phenomenon is modeled by mobility saturation at “high field”. We use a “High field saturation” model proposed by Canali et al.

The above models are implemented in ‘SemiVi’ drift-diffusion simulator and are activated throughout the device during the simulations.

III. MODELING TRAPPING AND DE-TRAPPING

During device operation, various trapping/de-trapping of electrons and holes take place simultaneously. Rates of these processes determine occupancy of the traps.

Occupancy of the trap levels depends on the rates of charging and discharging of the traps. Electron occupation factor f^n of the trap level is determined by net rate of capture of CB electrons r_C^n minus net rate of capture of VB holes r_V^p . This is given by,

$$\frac{\partial f^n}{\partial t} = r_C^n - r_V^p \quad (1a)$$

$$r_C^n = (1 - f^n) \cdot c_C^n - f^n \cdot e_C^n \quad (1b)$$

$$r_V^p = (1 - f^p) \cdot c_V^p - f^p \cdot e_V^p \quad (1c)$$

$$f^p = 1 - f^n \quad (1d)$$

In steady-state electron occupancy at a trap level f^n as follows.

$$f^n = \frac{c_C^n + e_V^p}{c_C^n + c_V^p + e_C^n + e_V^p} \quad (2)$$

A. Capture and emission rates

Capture and emission rates used in the above equation depend on various factors including trap energy level, carrier density, and the current density. Capture rate of an electron from the CB and that of a hole from the VB is given by,

$$c_C^n = \sigma_n \cdot (1 - g_n^J) \cdot v_{th}^n \cdot n \quad (3a)$$

$$c_V^p = \sigma_p \cdot (1 - g_p^J) \cdot v_{th}^p \cdot p \quad (3b)$$

Here, $\sigma_{n/p}$ are electron/hole capture cross-sections, v_{th}^n and v_{th}^p are thermal velocities of electron and hole. The model parameters $g_{n/p}^J$ determine proportionate contribution of n and of $|J_n|$ to the total capture rate.

$$e_C^n = \sigma_n \cdot v_{th}^n \cdot n1/g_n \quad (4a)$$

$$e_V^p = \sigma_p \cdot v_{th}^p \cdot p1/g_p \quad (4b)$$

$$n1 = N_C \exp\left(\frac{q(E_{trap} - E_C)}{kT}\right) \quad (4c)$$

$$p1 = N_V \exp\left(\frac{q(E_V - E_{trap})}{kT}\right) \quad (4d)$$

where, $g_{n/p}$ are degeneracy factors, E_{trap} is the trap energy level, and $N_{C/V}$ are CB and VB DOS.

When traps are used in the device, the above (de-)trapping processes are simulated in ‘SemiVi’ drift-diffusion simulator to calculate trap occupancy and the rates. When occupied, “donor” traps are neutral, else they are positively charged.

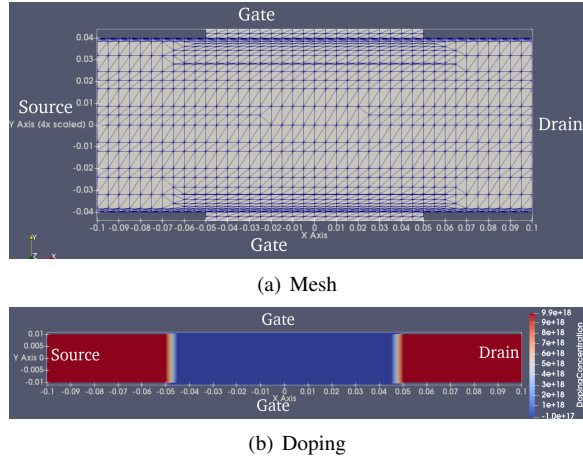


Fig. 1. Structure of the DG-MOSFET simulated in this paper - (a) mesh, (b) doping. Note, that mesh is stretched along y-axis by four for visualization purpose.

Similarly, when occupied, “acceptor” traps are negatively charged, else they are neutral. This charge state of the traps is taken into account in Poisson equation.

IV. SIMULATION SETUP

We use SemiVi ‘Structure generator and Mesher’ [?] to create the DG-MOSFET structure and mesh it using the built-in mesher.

A. Device Structure

The n-channel DG-MOSFET consists of a Silicon layer of thickness 20 nm and channel length of 100 nm. Source and drain of the device have 50nm length. Silicon layer is doped with Boron doping of $2 \times 10^{16}/\text{cm}^3$, while source/drain are doped with Phosphorus doping of $10^{19}/\text{cm}^3$.

In the p-channel DG-MOSFET, the Silicon channel is doped with Phosphorus doping of $2 \times 10^{16}/\text{cm}^3$, while the source and the drain are Boron doped with the doping of $10^{19}/\text{cm}^3$.

Gate-oxide is composed of SiO_2 with the thickness of 2nm on top and bottom of the stripe. Device structure and the doping concentration is shown in Fig. 1(b).

The device is meshed using ‘SemiVi’ mesher, which uses Quad-tree based ‘FEM meshing’. Since the channel region show sharp changes in electron density, mesh near gate-oxide/Si interface is refined. Final mesh is shown in Fig. 1(a).

Transfer characteristics of the n-channel (p-channel) MOSFET are simulated by quasistationarily ramping the gate voltage from 0V to 1V (-1V) at a constant drain voltage of 1V (-1V). SemiVi drift-diffusion simulator [?] is used for all the device simulations.

V. RESULTS AND DISCUSSION

A. Transfer characteristics

In the simulation of n-channel DG-MOSFET, donor type oxide/Silicon interface traps are simulated. The trap density (D_{it}) is varied from 0 to $6 \times 10^{12}/\text{cm}^2$ in the simulations. Transfer characteristics of the DG-MOSFET are plotted in

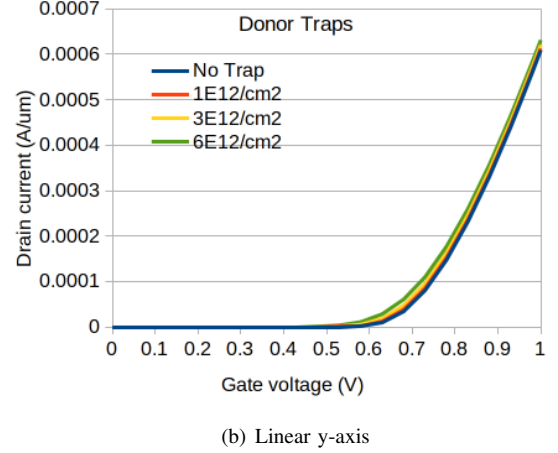
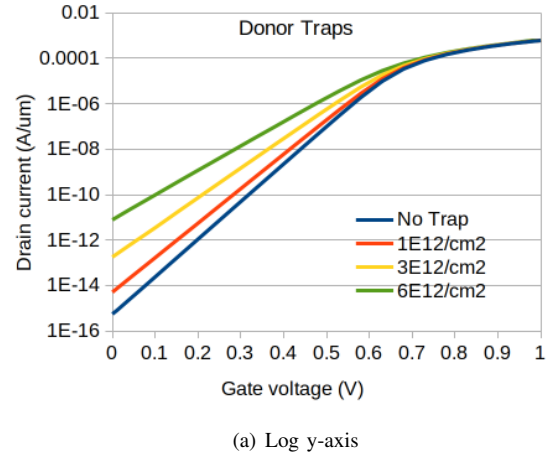
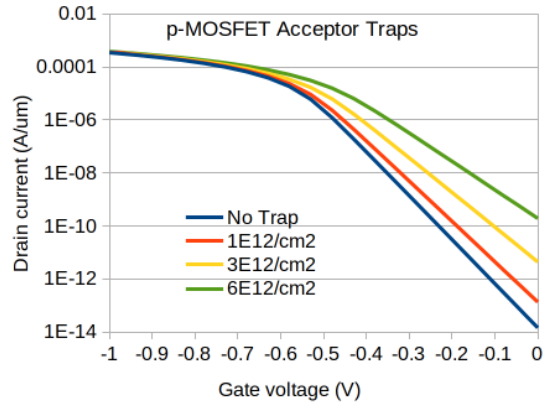


Fig. 2. Transfer characteristics of n-channel DG-MOSFET (a) log y-scale, (b) linear y-scale.

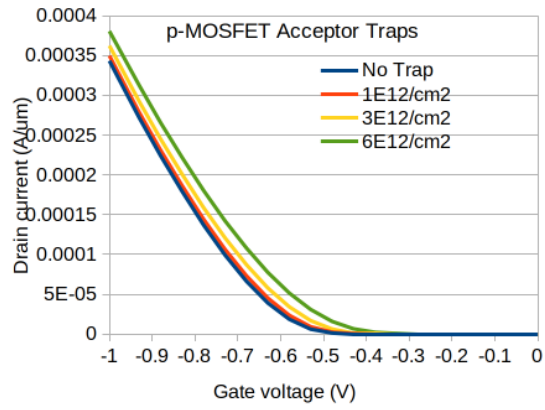
Fig. 2(a) at $V_{ds} = 1$ V. The plot shows, that as D_{it} increases, transfer characteristics become less steep in the subthreshold region. That is, subthreshold swing of the MOSFET increases. Transfer characteristics plotted in Fig. 2(b) confirm that on-state current is somewhat affected by increase of D_{it} .

Similarly, in the simulations of p-channel DG-MOSFET, acceptor-type oxide/Silicon interface traps are simulated. The trap density is varied from 0 to $6 \times 10^{12}/\text{cm}^2$ in the simulations. Transfer characteristics of the DG-MOSFET are plotted in Fig. 3(b) at $V_{ds} = -1$ V. The plot shows, that as D_{it} increases, subthreshold swing of the MOSFET increases. Transfer characteristics plotted in Fig. 3(a) confirm that on-state current is somewhat affected by the increase of D_{it} .

Reason for the increase of the subthreshold swing is, that increase of V_{gs} increases trap occupancy, thereby shielding the channel region from the gate voltage. This decreases gate coupling of the channel, and subthreshold swing increases.



(a) Log y-axis



(b) Linear y-axis

Fig. 3. Transfer characteristics of p-channel DG-MOSFET (a) log y-scale, (b) linear y-scale.